**TASK 0 Summary:**

The chip design flow begins with chip modeling, where a software application is developed in the C programming language and compiled to generate an initial output o0. This application is then run on a modeled processor architecture to verify the correctness of the instruction set implementation, producing output o1. Ensuring that o0 equals o1 serves as a checkpoint for freezing the design specifications.

Next is the RTL architecture stage, where the hardware is described using an HDL like Verilog. The same application is simulated on the RTL version of the processor, generating output o2. o2 should match o1. The synthesizable RTL is used to build digital blocks, while analog components like PLLs and ADCs are designed at the transistor level. These IPs are integrated into a complete SoC using buses and GPIOs. The application is run again to produce output o3, which must match the previous outputs to ensure correct system-level behavior.

The RTL to GDSII step involves backend processes such as floorplanning, PNR, clock tree synthesis. This step culminates in the generation of the GDSII file, the final layout sent for fabrication. In the physical verification and fabrication phase, the layout undergoes DRC and LVS checks. Once verified, the chip is manufactured referred to as tape out and enters the tape n phase where it is returned in physical form for testing.

The post-silicon validation stage involves placing the chip on an evaluation board and testing it with peripheral inputs to generate output o4. Confirming o4 matches all prior outputs ensures that the chip’s functionality has been preserved through every phase. Finally, in the system integration step, the validated chip is embedded into end-user products such as iwatches, arduino etc.